REMARKS

The present Amendment revises the title of the invention to make it more descriptive, as required in Section 2 of the Office Action. The new title is "Packet Communication Apparatus With First and Second Processing Circuits Which Access A Storage Circuit During First and Second Time Periods, Respectively."

The present Amendment also revises several of the claims to improve their form under US claim-drafting practice. Additionally, an unnecessary limitation is being deleted from the preambles of the independent claims (that the packets must have a "fixed-length").

Section 1 of the Office Action advises that an Information disclosure Statement that was filed with this application has not been considered. During a telephone conversation on or about April 18, 2003, the Examiner advised that he had not received the references. Accordingly, copies of the references are attached. Also attached is a copy of the prior law firm's filing receipt for the application and related papers (including the Information Disclosure Statement). It should be noted that the entry highlighted in color specifies three references, thereby providing evidence that they were present when the Information Disclosure Statement was filed. It would appear that they have simply gone astray at the Patent and Trademark Office.

The present application discloses an arrangement in which a packet processing time, representing the maximum time allowed for exchanging each packet, is divided into two parts as shown in Figure 2 of the application's drawings. During the first part, a first processing circuit for exchanging packets (that is, for transmitting and receiving packets) can access a storage circuit. During the second part of the packet processing time, representing the residue left over after the first part, a second processing circuit can access the storage circuit. For example, if the storage circuit is a DRAM, the processing performed by the second processing circuit may be a refresh operation.

The Office Action rejects all of the claims for anticipation or obviousness on the basis of patent 4,723,204 to Khera. The Khera reference discloses a computer arrangement in which a CPU periodically receives "hold" pulses so that refresh circuitry can refresh the computer's RAM in a time-sharing manner.

Claim 1 is directed to "a packet communication apparatus for processing consecutive fixed-length packets." The body of the claim recites a storage circuit and "a first processing circuit which accesses said storage circuit for executing first processing **with respect to data obtained from each of said packets**." In contrast, Khera's CPU is simply the CPU of a computer system, and there is nothing in the reference to suggest that it executes "processing with respect to data obtained from each of said packets." The word "packet" is not even present in the reference.

The body of claim 1 continues by reciting a second processing circuit and "an allocation circuit for executing access time allocation with respect to **a packet processing time allowed for processing each of said packets**, said allocation circuit allocating **a first time period of said packet processing time** to said first processing circuit for accessing said storage circuit and **a second time period of said packet processing time** to said second processing circuit for accessing said storage circuit...". The Khera reference, in contrast, does not split time periods that are allowed for processing packets. Instead, Khera teaches a brief refreshing period every 15 microseconds (see column 2, lines 19-26).

Accordingly, it is respectfully submitted that the invention defined by claim 1 is neither anticipated by Khera or rendered obvious by the reference. Since independent claim 8 contains language similar to that discussed above with respect to claim 1, it is respectfully submitted that it is also patentable.

The remaining claims depend from claim 1 and recite additional limitations to further define the invention. Accordingly, they are patentable along with claim1 and need not be further discussed. It is nevertheless noted that claims 3 and 5 recite "a producing circuit which receives a first packet synchronizing signal having first signal components

each **indicative of a boundary time point between adjacent packets** and produces a second packet synchronizing signal based on said first packet synchronizing signal...", and there is nothing in the Khera reference about packet synchronizing signals or boundary time points between adjacent packets.

For the foregoing reasons, it is respectfully submitted that the application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,

July 30, 2003
Date

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